FAIRCHILD SEMICONDUCTOR®

April 2009

FAN4800A/C, FAN4801/1S/2/2L PFC/PWM Controller Combination

Features

- Pin-to-Pin Compatible with ML4800 and FAN4800 and CM6800 and CM6800A
- PWM Configurable for Current-Mode or Feed-Forward Voltage-Mode Operation
- Internally Synchronized Leading-Edge PFC and Trailing-Edge PWM in one IC
- Low Operating Current
- Innovative *Switching-Charge* Multiplier Divider
- Average-Current-Mode for Input-Current Shaping
- PFC Over-Voltage and Under-Voltage Protections
- PFC Feedback Open-Loop Protection
- Peak Current Limiting for PFC
- Cycle-by-Cycle Current Limiting for PWM
- Power-On Sequence Control and Soft-Start
- Brownout Protection
- Interleaved PFC/PWM Switching
- FAN4801/1S/2/2L Improve Efficiency at Light Load
- f_{RTCT}=4•f_{PFC}=4•f_{PWM} for FAN4800A and FAN4801/1S
- f_{RTCT}=4•f_{PFC}=2•f_{PWM} for FAN4800C and FAN4802/2L

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- LCD TV, Monitor Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

Description

The highly integrated FAN4800A/C and FAN4801/1S/2/2L are specially designed for power supplies that consist of boost PFC and PWM. They require very few external components to achieve versatile protections / compensation. They are available in 16-pin DIP and SOP packages.

The PWM can be used in either current or voltage mode. In voltage mode, feed-forward from the PFC output bus can reduce the secondary output ripple.

Compared with older productions, ML4800 and FAN4800, FAN4800A/C and FAN4801/1S/2/2L have lower operation current that save power consumption in external devices. FAN4800A/C and FAN4801/1S/2/2L have accurate 49.9% maximum duty of PWM that makes the hold-up time longer. Specifically, the brownout protection and PFC soft-start functions are not in ML4800 and FAN4800.

To start evaluating FAN4800A/C, FAN4801/1S/2/2L for replacing existing FAN4800 and ML4800 boards, five things must be done before the fine-tuning procedure:

1. Change R_{AC} resister from the old value to a higher resister: between 6MΩ to 8MΩ.
2. Change RT/CT pin from the existing values to R_T=6.8KΩ and C_T=1000pF to have f_{PFC}=64KHz, f_{PWM}=64KHz.
3. VRMS pin needs to be 1.224V at V_{IN}=85 V_{AC} for universal input application from line input from 85V_{AC} to 270 V_{AC}. Both poles for the V_{rms} of FAN4801/1S/2/2L don't need to substantially slower than FAN4800; about 5 to 10 times.
4. At full load, the average V_{EA} needs to ~4.5V and the ripple on the V_{EA} needs to be less than 400mV.
5. Soft-Start pin, the soft-start current has been reduced to half from the FAN4800 capacitor.

Related Resources

Complete design instructions are detailed in application note AN-6078SC (available in Chinese only).

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN4800ANY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4800CNY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4800AMY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel
FAN4800CMY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel
FAN4801NY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4801SNY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4802NY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4802LNY	-40°C to +105°C	Green	16-pin Dual In-Line Package (DIP)	Tube
FAN4801MY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel
FAN4801SMY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel
FAN4802MY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel
FAN4802LMY	-40°C to +105°C	Green	16-pin Small Out-Line Package (SOP)	Tape and Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Part Number	PFC:PWM Frequency Ratio	Brown Out / In	Range In / Out
FAN4800ANY	1:1	1.05V / 1.9V	NA
FAN4800AMY	1:1	1.05V / 1.9V	NA
FAN4800CNY	1:2	1.05V / 1.9V	NA
FAN4800CMY	1:2	1.05V / 1.9V	NA
FAN4801NY	1:1	1.05V / 1.9V	1.95V / 2.45V
FAN4801SNY	1:1	1.05V / 1.9V	2.8V / 3.35V
FAN4802NY	1:2	1.05V / 1.9V	1.95V / 2.45V
FAN4802LNY	1:2	0.9V / 1.65V	1.95V / 2.45V
FAN4801MY	1:1	1.05V / 1.9V	1.95V / 2.45V
FAN4801SMY	1:1	1.05V / 1.9V	2.8V / 3.35V
FAN4802MY	1:2	1.05V / 1.9V	1.95V / 2.45V
FAN4802LMY	1:2	0.9V / 1.65V	1.95V / 2.45V

Application Diagram

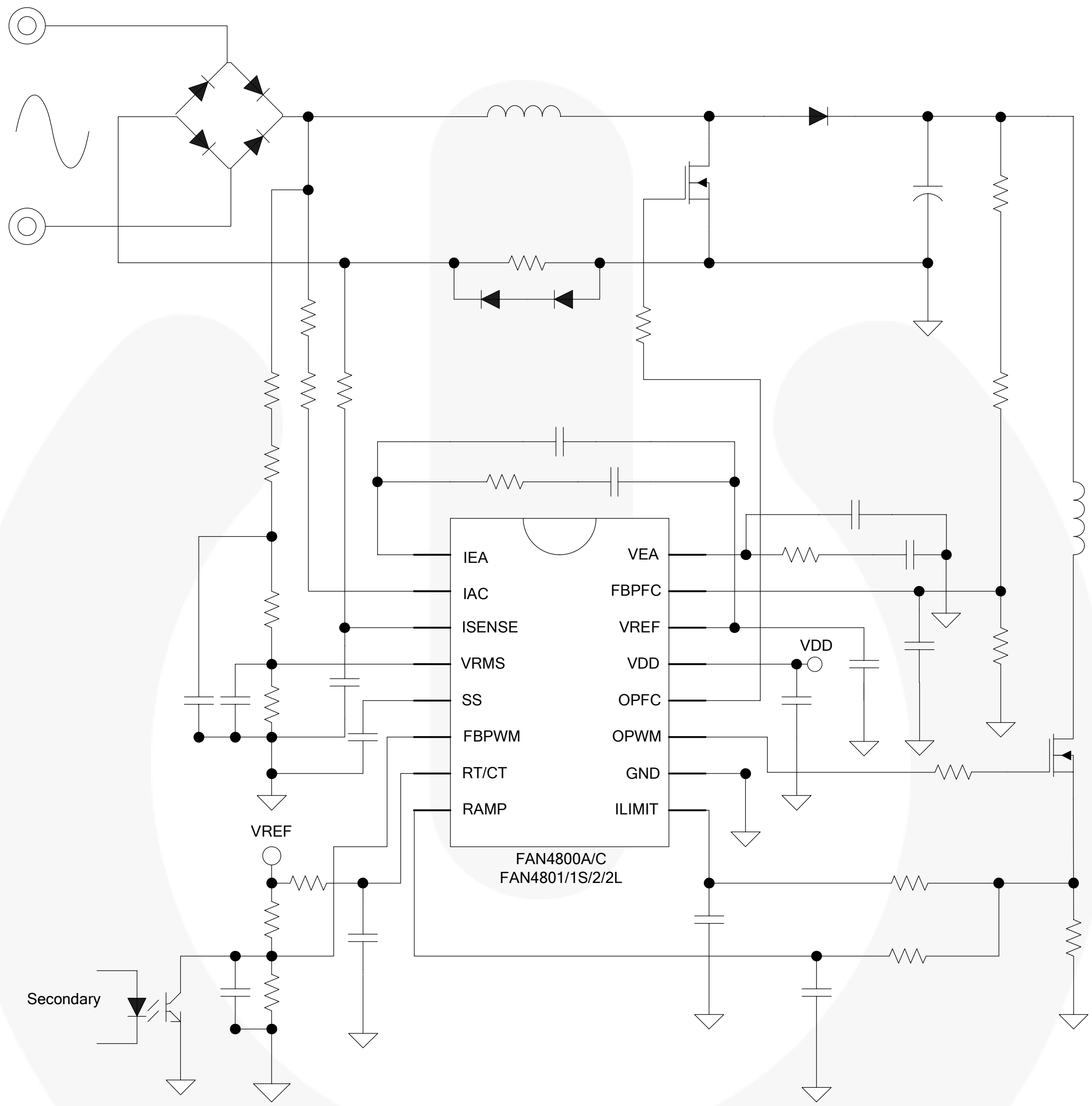


Figure 1. Typical Application Current Mode

Application Diagram

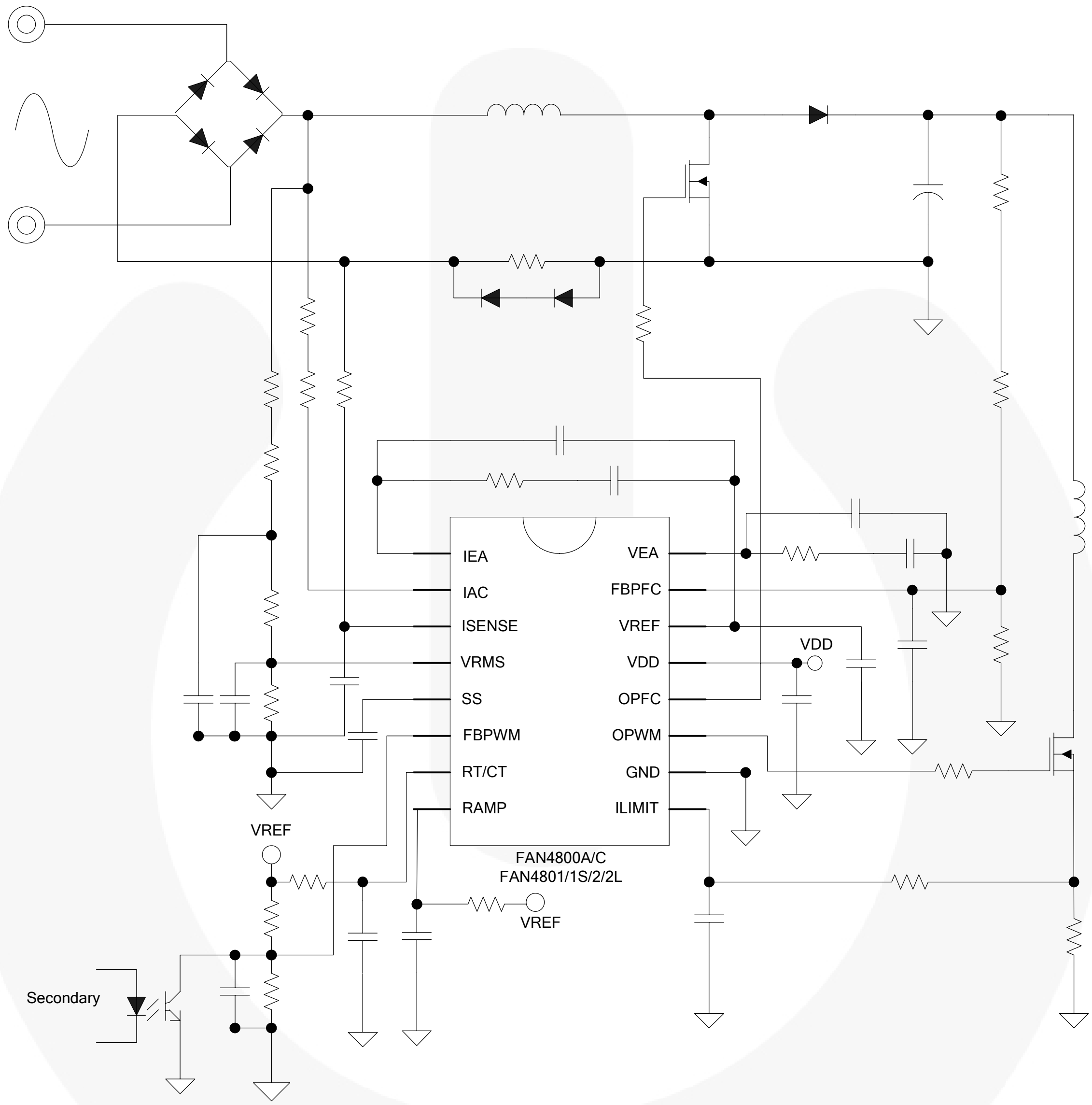


Figure 2. Typical Application Voltage Mode

Block Diagram

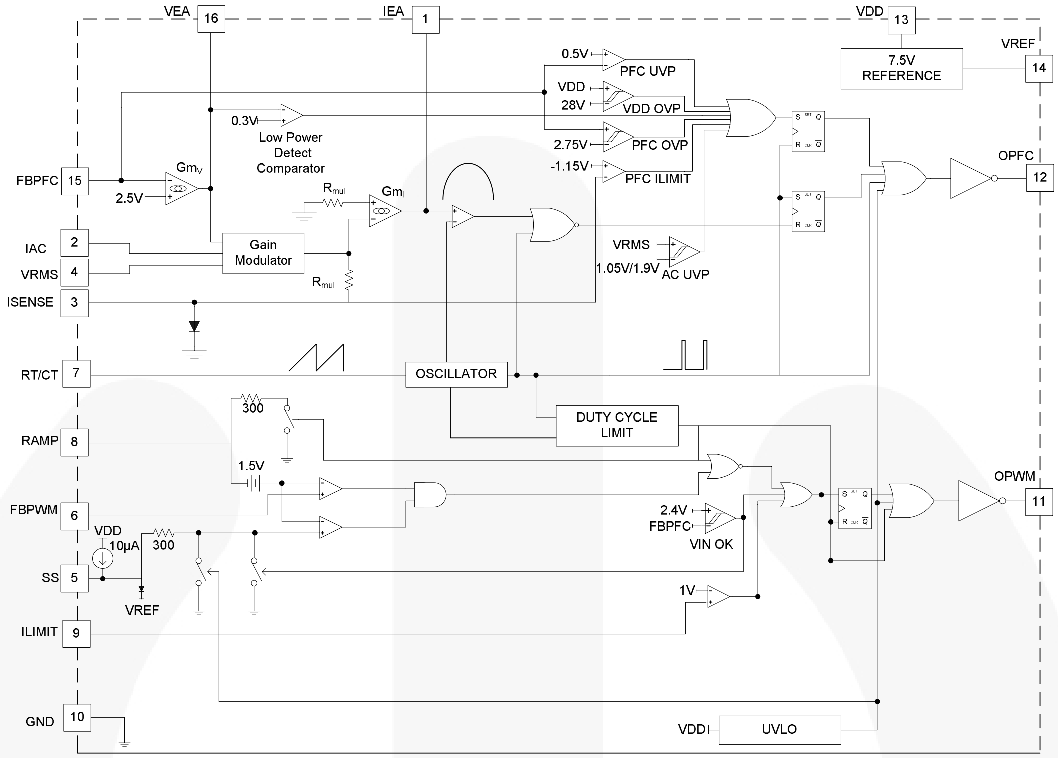


Figure 3. FAN4800A/C Function Block Diagram

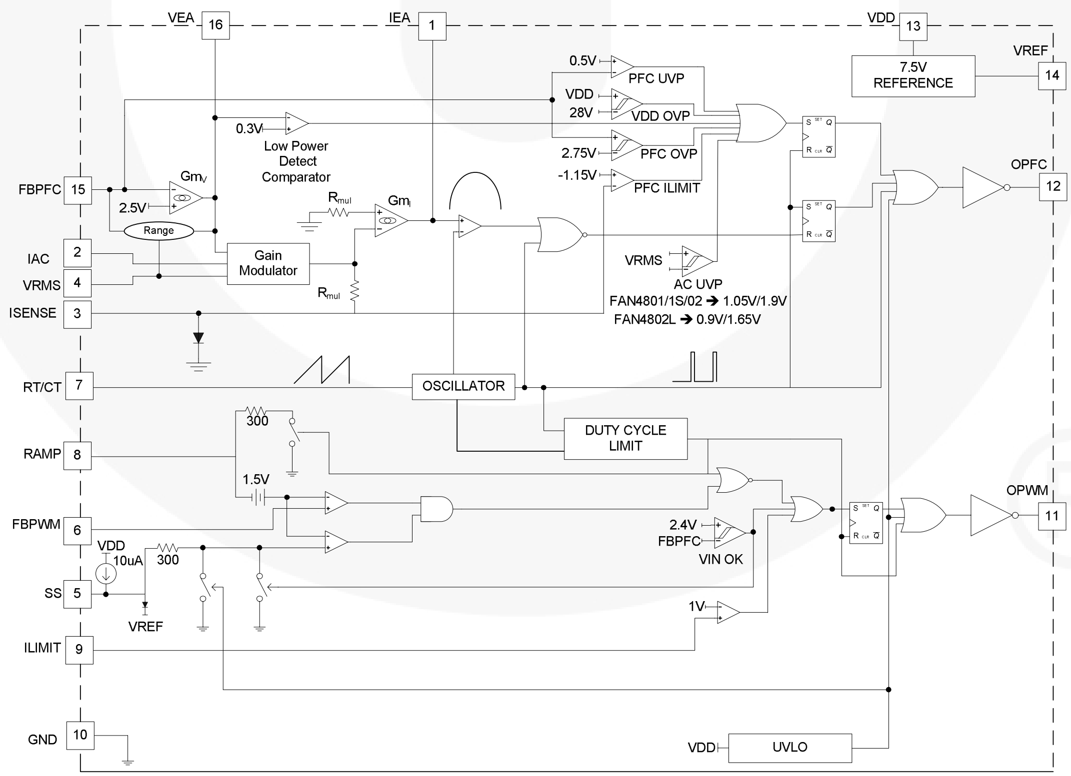
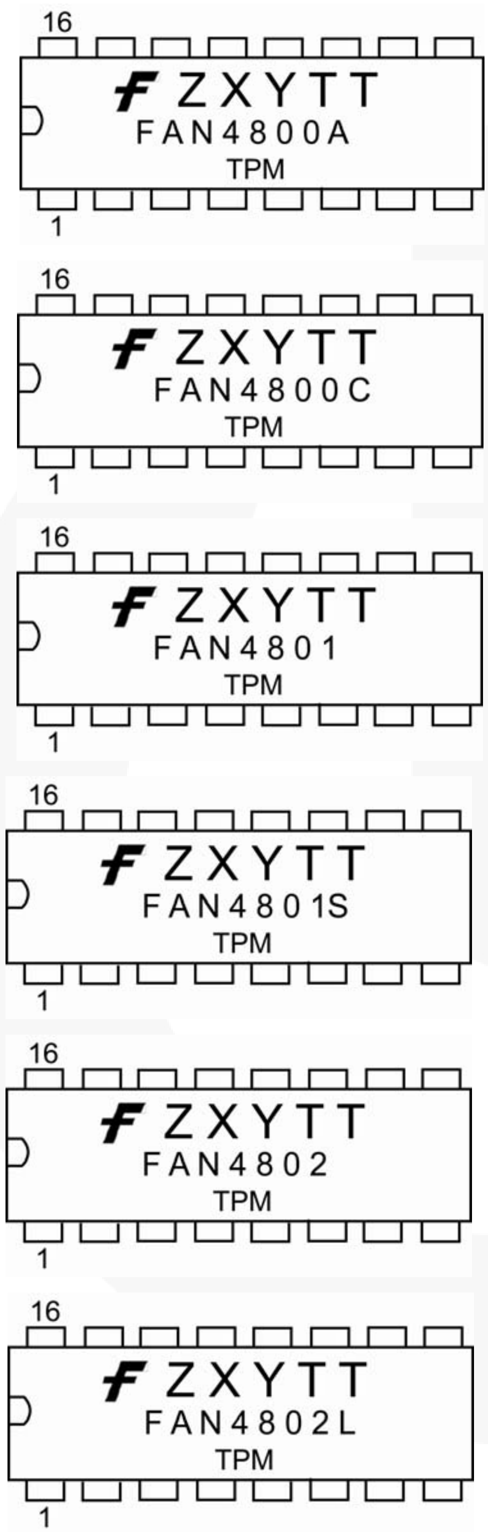


Figure 4. FAN4801/1S/2/2L Function Block Diagram

Marking Information



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die Run Code
T – Package Type (N:DIP, M:SOP)
P – Y: Green Package
M – Manufacture Flow Code

Figure 5. Top Mark

Pin Configuration

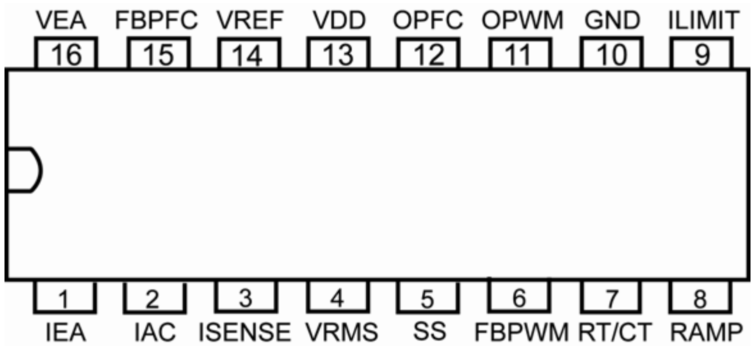


Figure 6. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	IEA	**Output of PFC Current Amplifier**. The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive.
2	IAC	**Input AC Current**. For normal operation, this input provides current reference for the multiplier. The suggested maximum IAC is 100µA.
3	ISENSE	**PFC Current Sense**. The non-inverting input of the PFC current amplifier and the output of multiplier and PFC ILIMIT comparator.
4	VRMS	**Line-Voltage Detection**. Line voltage detection. The pin is used for PFC multiplier.
5	SS	**PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 10µA constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or PWM disabled, the SS pin is quickly discharged.
6	FBPWM	**PWM Feedback Input**. The control input for voltage-loop feedback of PWM stage.
7	RT/CT	**Oscillator RC Timing Connection**. Oscillator timing node; timing set by R_T and C_T.
8	RAMP	**PWM RAMP Input**. In current mode, this pin functions as the current sense input; when in voltage mode, it is the feed forward sense input from PFC output 380V (feedforward ramp).
9	ILIMIT	**Peak Current Limit Setting for PWM**. The peak current limits setting for PWM.
10	GND	**Ground**.
11	OPWM	**PWM Gate Drive**. The totem-pole output drive for PWM MOSFET. This pin is internally clamped under 15V to protect the MOSFET.
12	OPFC	**PFC Gate Drive**. The totem pole output drive for PWM MOSFET. This pin is internally clamped under 15V to protect the MOSFET.
13	VDD	**Supply**. The power supply pin. The threshold voltages for startup and turn-off are 11V and 9.3V, respectively. The operating current is lower than 10mA.
14	VREF	**Reference Voltage**. Buffered output for the internal 7.5V reference.
15	FBPFC	**Voltage Feedback Input for PFC**. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
16	VEA	**Output of PFC Voltage Amplifier**. The error amplifier output for PFC voltage feedback loop. A compensation network is connected between this pin and ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			30	V
V_H	SS, FBPWM, RAMP, OPWM, OPFC		-0.3	30.0	V
V_L	IAC, VRMS, RT/CT, ILIMIT, FBPFC, VEA		-0.3	7.0	V
V_{VREF}	VREF			7.5	V
V_{IEA}	IEA		0	V_{VREF}+0.3	V
V_N	ISENSE		-5.0	0.7	V
I_{AC}	Input AC Current			1	mA
I_{REF}	V_{REF} Output Current			5	mA
$I_{PFC\text{-}OUT}$	Peak PFC OUT Current, Source or Sink			0.5	A
$I_{PWM\text{-}OUT}$	Peak PWM OUT Current, Source or Sink			0.5	A
P_D	Power Dissipation T_A < 50°C			800	mW
$R_{\Theta\ j\text{-}a}$	Thermal Resistance (Junction-to-Air)	DIP		80.80	°C/W
		SOP		104.10	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature(Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4.5	kV
		Charged Device Model, JESD22-C101		1000	V

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under “absolute maximum ratings “may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25°C, R_T=6.8kΩ, C_T=1000pF unless noted operating specifications.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD Section						
$I_{DD\ ST}$	Startup Current	V_{DD}=V_{TH-ON}-0.1V; OPFC OPWM Open		30	80	µA
I_{DD-OP}	Operating Current	V_{DD}=13V; OPFC OPWM Open	2.0	2.6	5.0	mA
V_{TH-ON}	Turn-On Threshold Voltage		10	11	12	V
ΔV_{TH}	Hysteresis		1.5		1.9	V
V_{DD-OVP}	V_{DD} OVP		27	28	29	V
ΔV_{DD-OVP}	V_{DD} OVP Hysteresis			1		V
Oscillator						
$f_{OSC-RT/CT}$	RT/CT Frequency	R_T=6.8kΩ, C_T=1000pF	240	256	268	kHz
f_{OSC}	PFC & PWM Frequency	R_T=6.8kΩ, C_T=1000pF	60	64	67	kHz
	FAN4800C,FAN4802/02L PWM Frequency		120	128	134	
f_{DV}	Voltage Stability	11V ≦ V_{DD} ≦ 22V			2	%
f_{DT}	Temperature Stability	-40°C ~ +105°C			2	%
f_{TV}	Total Variation (PFC & PWM)(3)	Line, Temperature	58		70	kHz
f_{RV}	Ramp Voltage(3)	Valley to Peak		2.8		V
$I_{Discharge}$	Discharge Current	V_{RAMP}=0V, $V_{RT/CT}$=2.5V	6.5		15	mA
f_{RANGE}	Frequency Range(3)		50		75	kHz
t_{PFCD}	PFC Dead Time	R_T=6.8kΩ, C_T=1000pF	400	600	800	ns
VREF						
V_{VREF}	Reference Voltage	I_{REF}=0mA, C_{REF}=0.1µF	7.4	7.5	7.6	V
ΔV_{VREF1}	Load Regulation of Reference Voltage	C_{REF}=0.1µF, I_{REF}=0mA to 3.5mA V_{VDD}=14V, Rise/Fall Time > 20µs		30	50	mV
ΔV_{VREF2}	Line Regulation of Reference Voltage	C_{REF}=0.1µF, V_{VDD}=11V to 22V			25	mV
$\Delta V_{VREF-DT}$(3)	Temperature Stability	-40°C ~ +105°C		0.4	0.5	%
$\Delta V_{VREF-TV}$(3)	Total Variation	Line, Load, Temp	7.35		7.65	V
$\Delta V_{VREF-LS}$(3)	Long-Term Stability	T_J=125°C, 0 ~ 1000HRs	5		25	mV
$I_{REF-MAX.}$	Maximum Current	V_{VREF} > 7.35V	5			mA
I_{OS}(3)	Output Short Circuit			25		mA
PFC OVP Comparator						
$V_{PFC-OVP}$	Over-Voltage Protection		2.70	2.75	2.80	V
$\Delta V_{PFC-OVP}$	PFC OVP Hysteresis		200	250	300	mV
Low-Power Detect Comparator						
V_{EAOFF}	VEA Voltage OFF OPFC		0.2	0.3	0.4	V
V_{IN} OK Comparator						
$V_{RD-FBPFC}$	Voltage Level on FBPFC to Enable OPWM During Startup		2.3	2.4	2.5	V
$\Delta V_{RD-FBPFC}$	Hysteresis		1.15	1.25	1.35	V

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C, R_T=6.8kΩ, C_T=1000pF unless noted operating specifications.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier						
FBPFC	Input Voltage Range(3)		0		6	V
V_{ref}	Reference Voltage	at T=25°C	2.45	2.50	2.55	V
A_V	Open-Loop Gain(3)		35	42		dB
Gm_v	Transconductance	V_{NONINV}=V_{INV}, V_{VEA}=3.75V at T=25°C	50	70	90	μmho
$I_{FBPFC-L}$	Maximum Source Current	V_{FBPFC}=2V, V_{VEA}=1.5V	40	50		μA
$I_{FBPFC-H}$	Maximum Sink Current	V_{FBPFC}=3V, V_{VEA}=6V		-50	-40	μA
I_{BS}	Input Bias Current		-1		1	μA
V_{VEA-H}	Output High Voltage on VVEA		5.8	6.0		V
V_{VEA-L}	Output Low Voltage on VVEA			0.1	0.4	V
Current Error Amplifier						
V_{ISENSE}	Input Voltage Range (ISENSE Pin)(3)		-1.5		0.7	V
Gm_I	Transconductance	V_{NONINV}=V_{INV}, V_{IEA}=3.75V	78	88	100	μmho
V_{OFFSET}	Input Offset Voltage	V_{VEA}=0V, IAC Open	-10		10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	8.0	V
V_{IEA-L}	Output Low Voltage			0.1	0.4	V
I_L	Source Current	V_{ISENSE}=-0.6V, V_{IEA}=1.5V	35	50		μA
I_H	Sink Current	V_{ISENSE}=+0.6V, V_{IEA}=4.0V		-50	-35	μA
A_I	Open-Loop Gain(3)		40	50		dB
Tri-Fault Detect						
t_{FBPFC_OPEN}	Time to FBPFC Open(3)	V_{FBPFC}=$V_{PFC-UVP}$ to FBPFC OPEN, 470pF from FBPFC to GND		2	4	ms
$V_{PFC-UVP}$	PFC Feedback Under-Voltage Protection		0.4	0.5	0.6	V
Gain Modulator						
I_{AC}	Input for AC Current(3)	Multiplier Linear Range	0		100	μA
GAIN	GAIN Modulator(4)	I_{AC}=17.67μA, V_{RMS}=1.080V V_{FBPFC}=2.25V, at T=25°C	7.50	9.00	10.50	
		I_{AC}=20μA, V_{RMS}=1.224V V_{FBPFC}=2.25V, at T=25°C	6.30	7.00	7.70	
		I_{AC}=25.69μA, V_{RMS}=1.585V V_{FBPFC}=2.25V, at T=25°C	3.80	4.20	4.60	
		I_{AC}=51.62μA, V_{RMS}=3.169V V_{FBPFC}=2.25V, at T=25°C	0.95	1.05	1.16	
		I_{AC}=62.23μA, V_{RMS}=3.803V V_{FBPFC}=2.25V, at T=25°C	0.66	0.73	0.80	
BW	Bandwidth(3)	I_{AC}=40μA		2		kHz
$V_{o(gm)}$	Output Voltage=5.7kΩ × (I_{SENSE}-I_{OFFSET})(3)	I_{AC}=20μA, V_{RMS}=1.224V V_{FBPFC}=2.25V, at T=25°C	0.74	0.82	0.90	V

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C, R_T=6.8kΩ, C_T=1000pF unless noted operating specifications.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PFC ILIMIT Comparator						
$V_{PFC\text{-}ILIMIT}$	Peak Current Limit Threshold Voltage, Cycle-by-Cycle Limit		-1.25	-1.15	-1.05	V
ΔV_{pk}	PFC ILIMIT-Gain Modulator Output	I_{AC}=17.67µA, V_{RMS}=1.08V V_{FBPFC}=2.25V, at T=25°C	200			mV
PFC Output Driver						
$V_{GATE\text{-}CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V	13	15	17	V
$V_{GATE\text{-}L}$	Gate Low Voltage	V_{DD}=15V; I_O=100mA			1.5	V
$V_{GATE\text{-}H}$	Gate High Voltage	V_{DD}=13V; I_O=100mA	8			V
t_r	Gate Rising Time	V_{DD}=15V; C_L=4.7nF; O/P=2V to 9V	40	70	120	ns
t_f	Gate Falling Time	V_{DD}=15V; C_L=4.7nF; O/P=9V to 2V	40	60	110	ns
$D_{PFC\text{-}MAX}$	Maximum Duty Cycle	V_{IEA}<1.2V	94	97		%
$D_{PFC\text{-}MIN}$	Minimum Duty Cycle	V_{IEA}>4.5V			0	%
Brown Out						
$V_{RMS\text{-}UVP}$	V_{RMS} Threshold Low	FAN4800A/C, FAN4801/1S/2	1.00	1.05	1.10	V
		FAN4802L	0.85	0.90	0.95	V
$V_{RMS\text{-}UVP}$	V_{RMS} Threshold High	FAN4800A/C, FAN4801/1S/2	1.85	1.90	1.95	V
		FAN4802L	1.60	1.65	1.70	V
$\Delta V_{RMS\text{-}UVP}$	Hysteresis	FAN4800A/C, FAN4801/1S/2	750	850	950	mV
		FAN4802L	650	750	850	mV
t_{UVP}	Under-Voltage Protection Delay Time		340	410	480	ms
Soft-Start						
$V_{SS\text{-}MAX}$	Maximum Voltage	V_{DD}=15V	9.5	10.0	10.5	V
I_{SS}	Soft-Start Current			10		µA
PWM ILIMIT Comparator						
$V_{PWM\text{-}ILIMIT}$	Threshold Voltage		0.95	1.00	1.05	V
t_{PD}	Delay to Output			250		ns
$t_{PWM\text{-}Bnk}$	Leading-Edge Blanking Time		170	250	350	ns
Range (FAN4801/1S/2/2L)						
$V_{RMS\text{-}L}$	RMS AC Voltage LOW	When V_{RMS}=1.95V at 132V_{RMS}	1.90	1.95	2.00	V
$V_{RMS\text{-}H}$	RMS AC Voltage HIGH	When V_{RMS}=2.45V at 150V_{RMS}	2.40	2.45	2.50	V
$V_{EA\text{-}L}$	VEA LOW	When V_{VEA}=1.95V at 30% Loading,	1.90	1.95	2.00	V
	VEA LOW (FAN4801S)	When V_{VEA}=2.80V at 60% Loading	2.75	2.80	2.85	
$V_{EA\text{-}H}$	VEA HIGH	When V_{VEA}=2.45V at 40% Loading,	2.40	2.45	2.50	V
	VEA HIGH (FAN4801S)	When V_{VEA}=3.35V at 70% Loading	3.30	3.35	3.40	
I_{tc}	Two-Level Current	FBPFC Two-Level Current	18	20	22	µA

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C, R_T=6.8kΩ, C_T=1000pF unless noted operating specifications.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM Output Driver						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V	13	15	17	V
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V; I_O=100mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=13V; I_O=100mA	8			V
t_r	Gate Rising Time	V_{DD}=15V; C_L=4.7nF	30	60	120	ns
t_f	Gate Falling Time	V_{DD}=15V; C_L=4.7nF	30	50	110	ns
$D_{PWM-MAX}$	Maximum Duty Cycle		49.0	49.5	50.0	%
V_{PWM-LS}	PWM Comparator Level Shift		1.3	1.5	1.8	V

Notes:

3. This parameter, although guaranteed by design, is not 100% production tested.
4. Gain=K × 5.3 × $(V_{RMS}^2)^{-1}$; K=(I_{SENSE} − I_{OFFSET}) × $[I_{AC} \times (V_{EA} - 0.7V)]^{-1}$; $V_{EA\ (MAX.)}$=5.6V.

Typical Characteristics

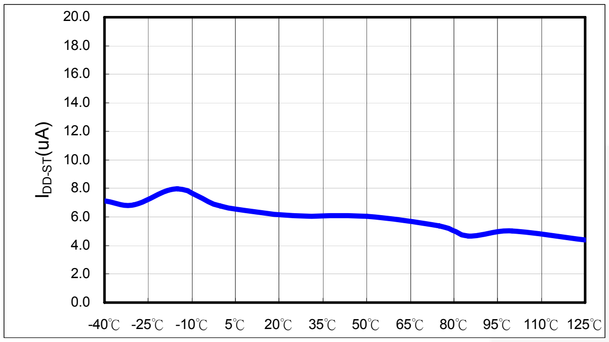


Figure 7. $I_{DD\text{-}ST}$ vs. Temperature

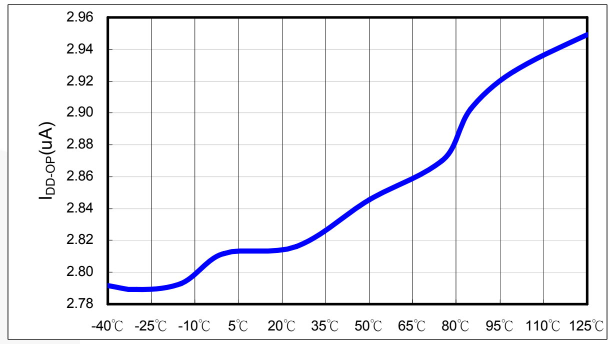


Figure 8. $I_{DD\text{-}OP}$ vs. Temperature

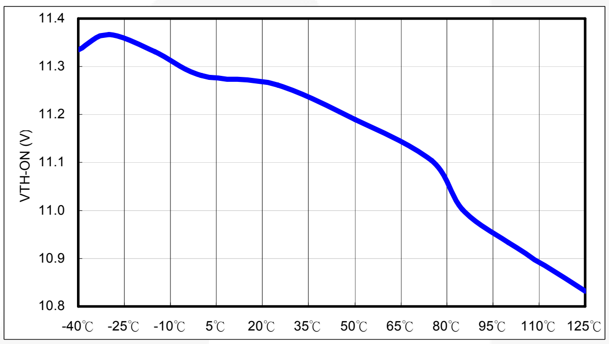


Figure 9. $V_{TH\text{-}ON}$ vs. Temperature

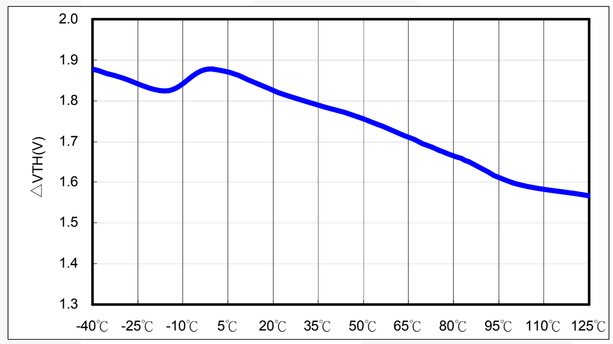


Figure 10. ΔV_{TH} vs. Temperature

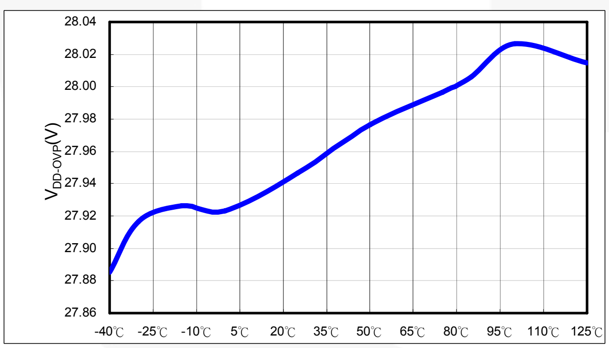


Figure 11. $V_{DD\text{-}OVP}$ vs. Temperature

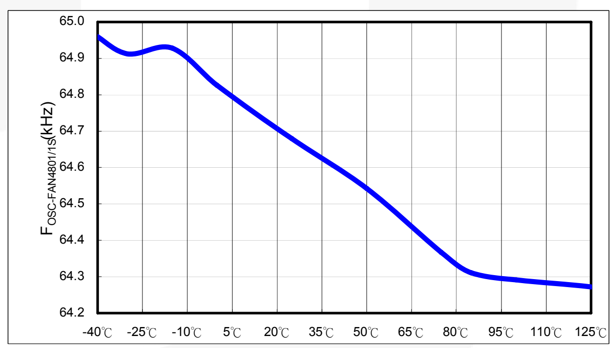


Figure 12. $f_{OSC\text{-}FAN4801/1S}$ vs. Temperature

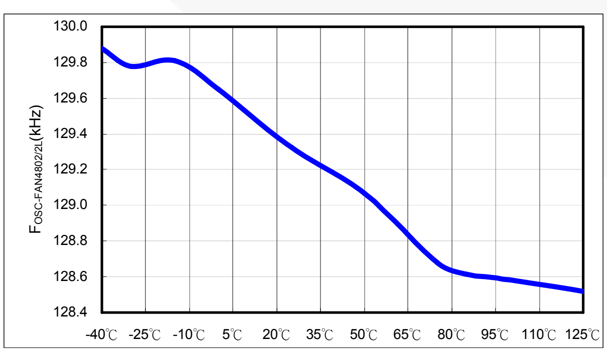


Figure 13. $f_{OSC\text{-}FAN4802/2L}$ vs. Temperature

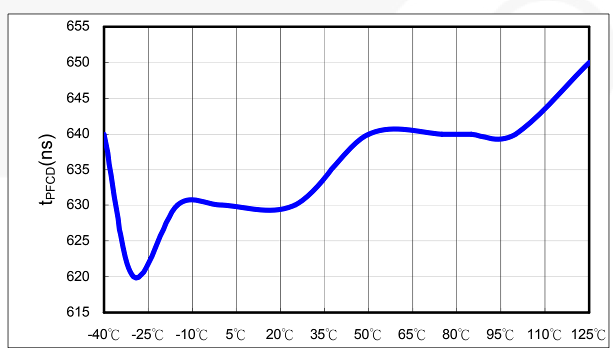


Figure 14. t_{PFCD} vs. Temperature

Typical Characteristics

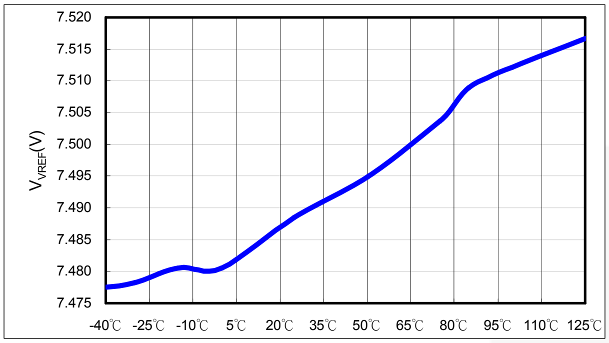


Figure 15. V_{VREF} vs. Temperature

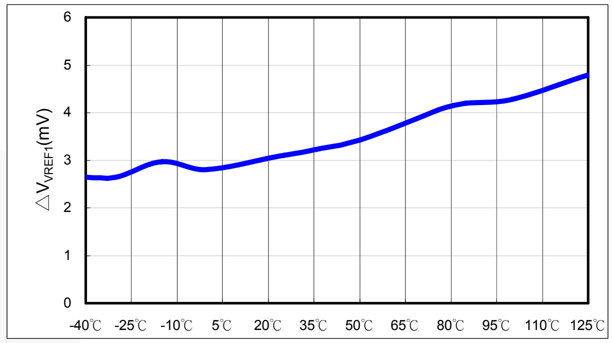


Figure 16. ΔV_{VREF1} vs. Temperature

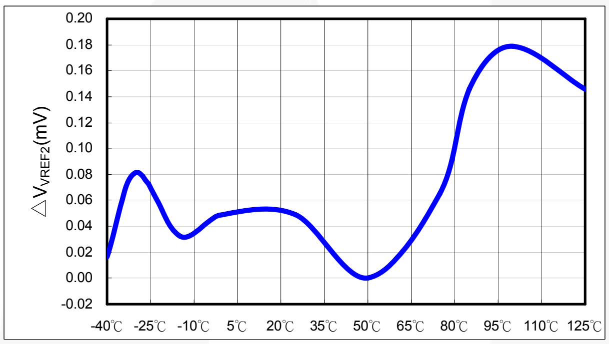


Figure 17. ΔV_{VREF2} vs. Temperature

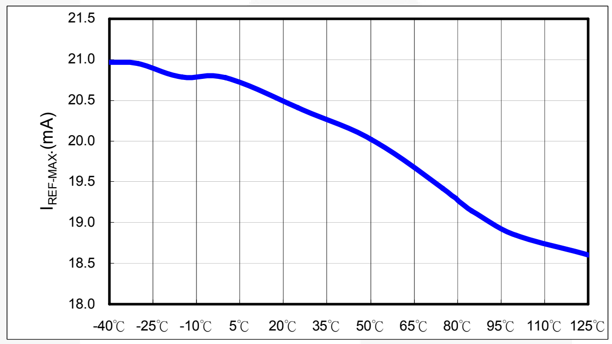


Figure 18. $I_{REF-MAX.}$ vs. Temperature

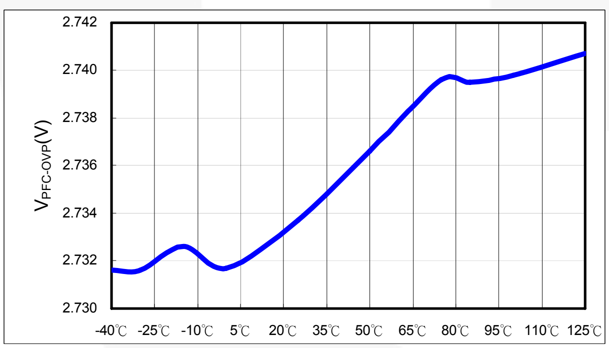


Figure 19. $V_{PFC-OVP}$ vs. Temperature

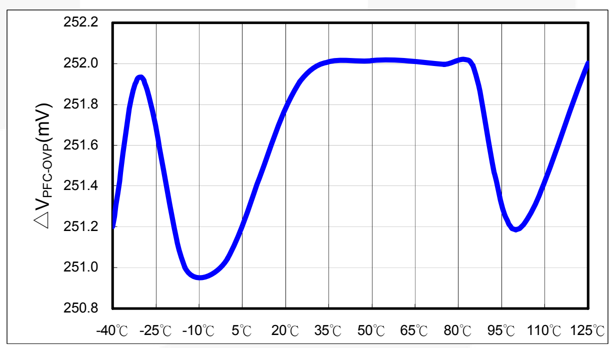


Figure 20. $\Delta V_{PFC-OVP}$ vs. Temperature

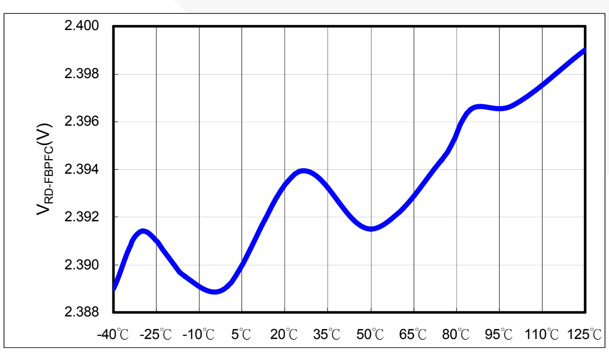


Figure 21. $V_{RD-FBPFC}$ vs. Temperature

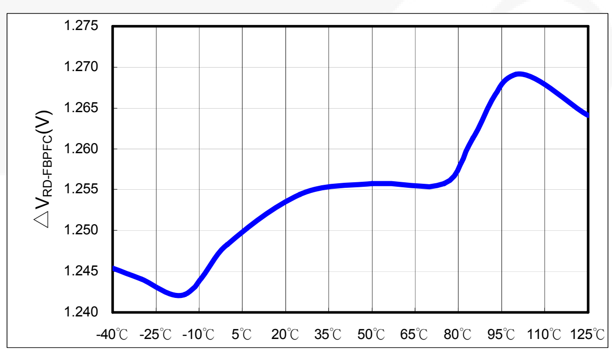


Figure 22. $\Delta V_{RD-FBPFC}$ vs. Temperature

Typical Characteristics

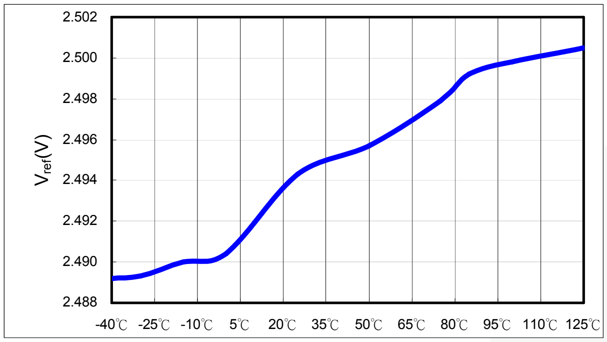


Figure 23. V_{REF} vs. Temperature

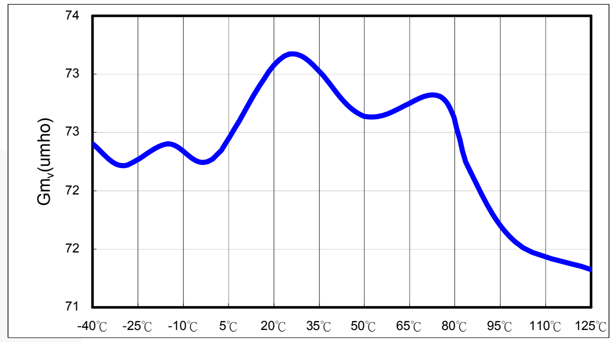


Figure 24. Gm_V vs. Temperature

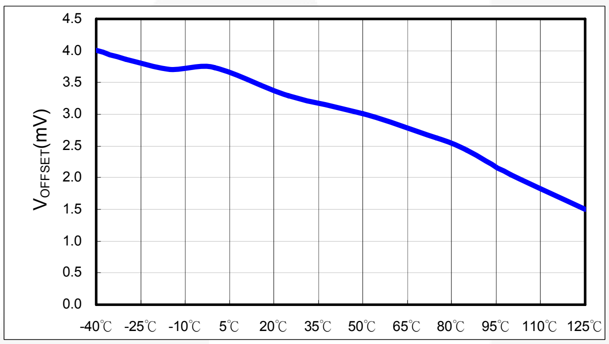


Figure 25. V_{OFFSET} vs. Temperature

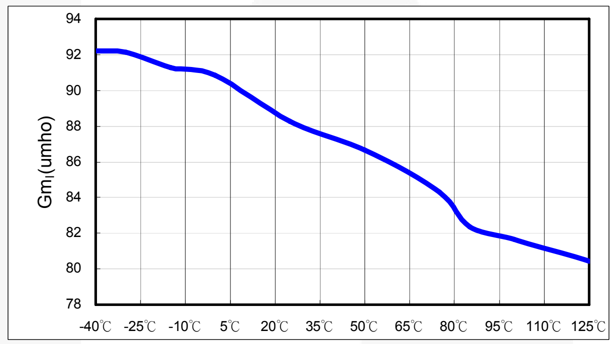


Figure 26. Gm_I vs. Temperature

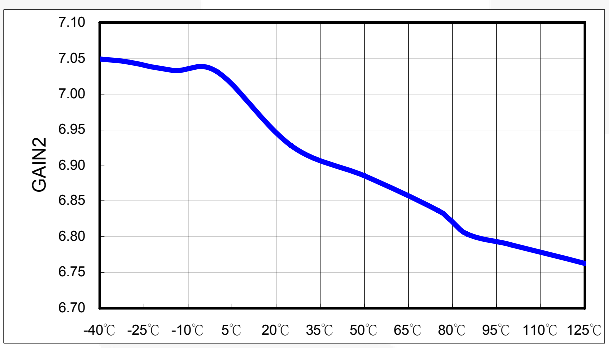


Figure 27. GAIN2 vs. Temperature

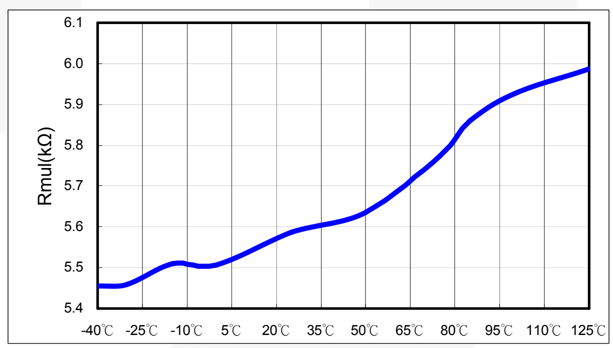


Figure 28. Rmul vs. Temperature

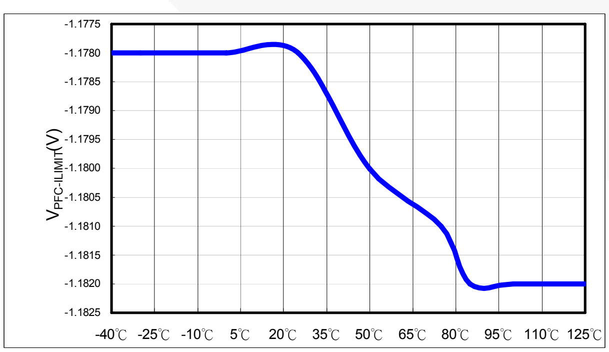


Figure 29. $V_{PFC\text{-}ILIMIT}$ vs. Temperature

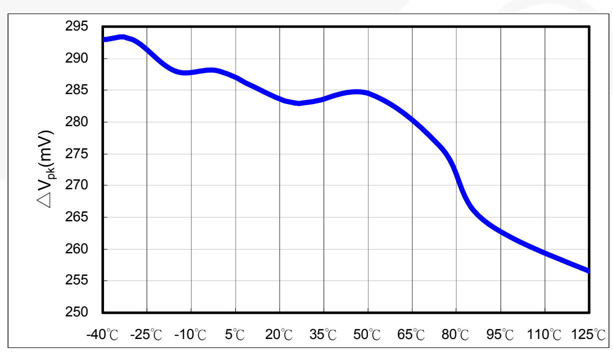


Figure 30. ΔV_{pk} vs. Temperature

Typical Characteristics

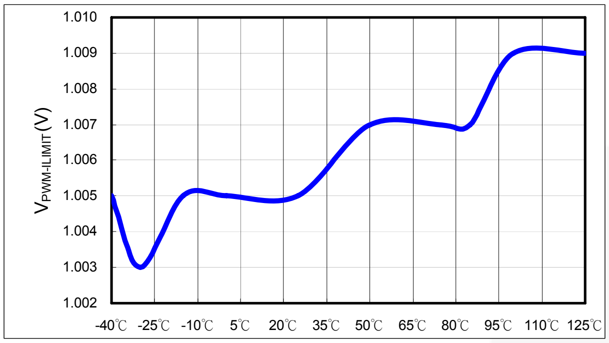


Figure 31. $V_{PWM-ILIMIT}$ vs. Temperature

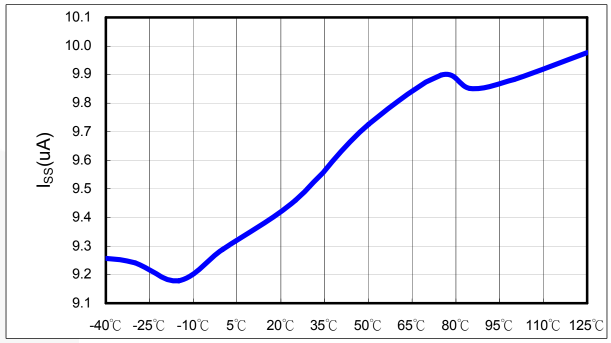


Figure 32. I_{SS} vs. Temperature

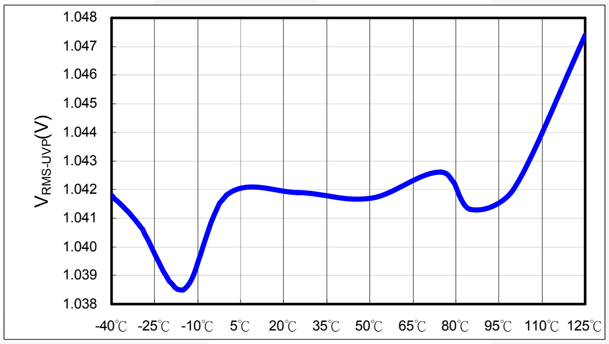


Figure 33. $V_{RMS-UVP}$ vs. Temperature

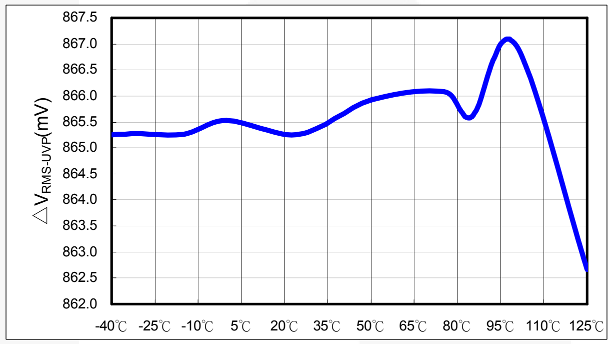


Figure 34. $\Delta V_{RMS-UVP}$ vs. Temperature

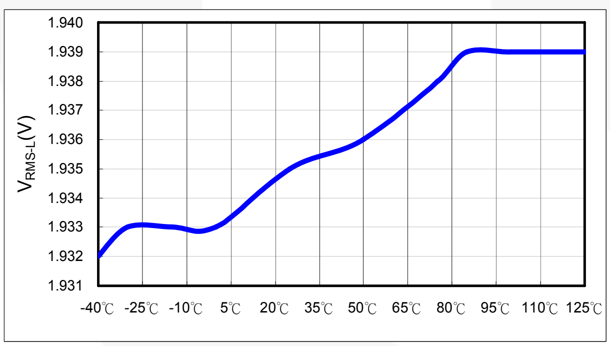


Figure 35. V_{RMS-L} vs. Temperature

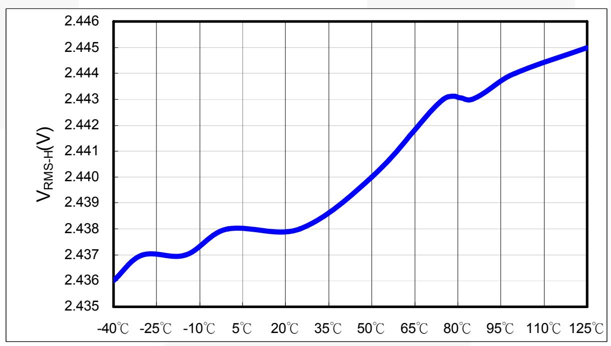


Figure 36. V_{RMS-H} vs. Temperature

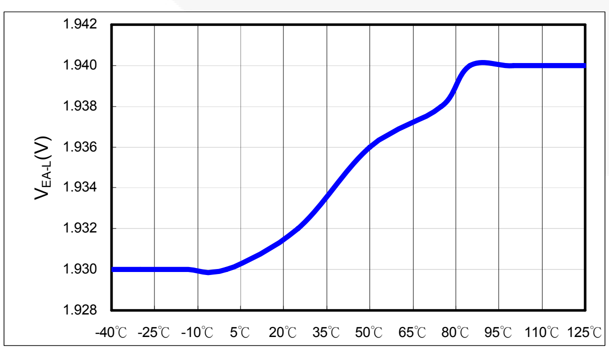


Figure 37. V_{EA-L} vs. Temperature

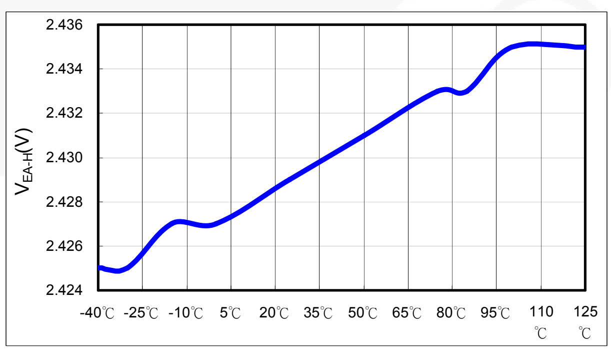


Figure 38. V_{EA-H} vs. Temperature

Typical Characteristics

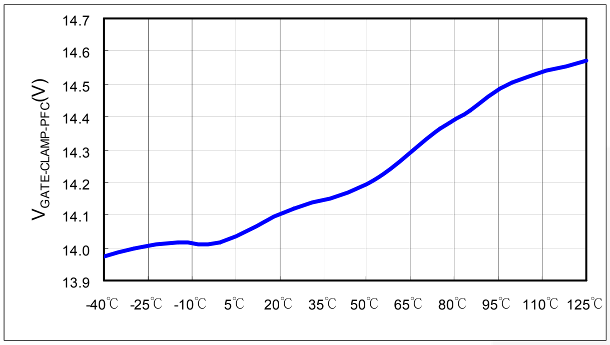


Figure 39. $V_{GATE-CLAMP-PFC}$ **vs. Temperature**

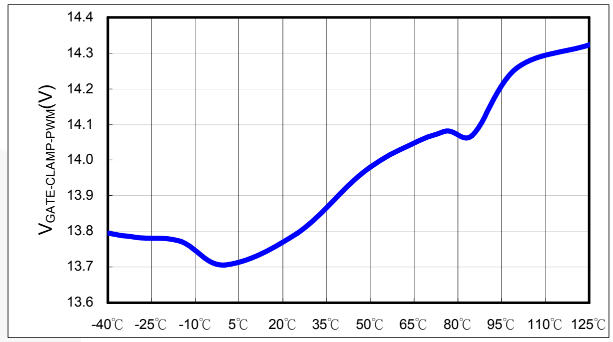


Figure 40. $V_{GATE-CLAMP-PWM}$ **vs. Temperature**

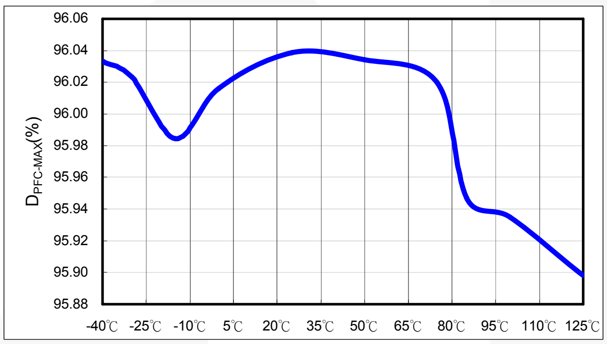


Figure 41. $D_{PFC-MAX}$ **vs. Temperature**

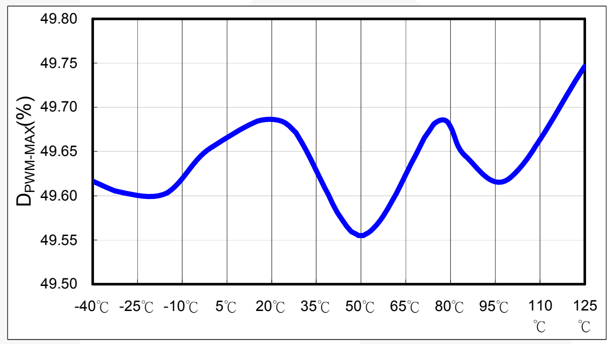


Figure 42. $D_{PWM-MAX}$ **vs. Temperature**

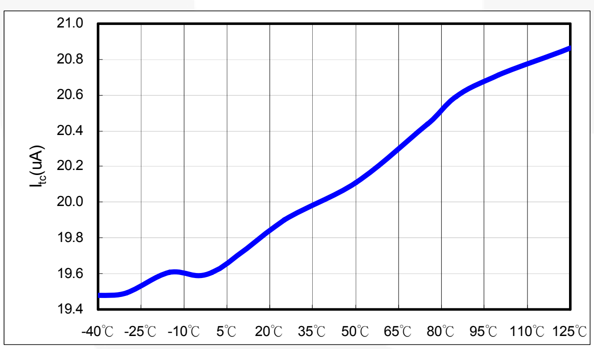


Figure 43. I_{tc} **vs. Temperature**

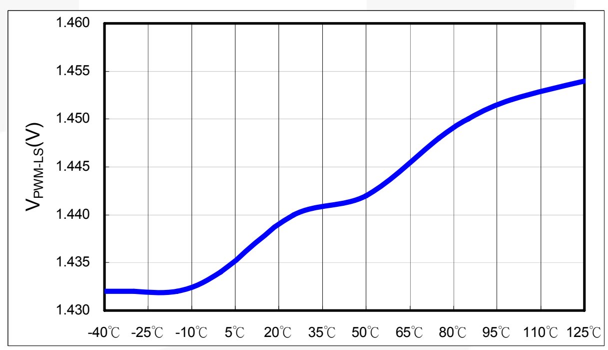


Figure 44. V_{PWM-LS} **vs. Temperature**

Functional Description

The FAN4800A/C and FAN4801/1S/2/2L consist of an average current controlled, continuous boost Power Factor Correction (PFC) front-end and a synchronized Pulse Width Modulator (PWM) back-end. The PWM can be used in current or voltage mode. In voltage mode, feed forward from the PFC output bus can be used to improve the line regulation of PWM. In either mode, the PWM stage uses conventional trailing-edge, duty-cycle modulation. This proprietary leading/trailing edge modulation results in a higher usable PFC error amplifier bandwidth and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the FAN4800A, FAN4801/1S operates at the same frequency as the PFC; and FAN4800C, FAN4802/2L operates at double with PFC.

In addition to power factor correction, a number of protection features are built into this series. They include soft-start, PFC over-voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout (UVLO).

Gain Modulator

The gain modulator is the heart of the PFC, as the circuit block controls the response of the current loop to line voltage waveform and frequency, RMS line voltage, and PFC output voltages. There are three inputs to the gain modulator:

1. A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is fed into the gain modulator at IAC. Sampling current in this way minimizes ground noise, required in high-power, switching-power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The output of the gain modulator is inversely proportional to V_{RMS} (except at unusually low values of V_{RMS}, where special gain contouring takes over to limit power dissipation of the circuit components under brownout conditions).
3. The output of the voltage error amplifier, V_{EA}. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual ground (negative) input of the current error amplifier. In this way, the gain modulator forms the reference for the current error loop and ultimately controls the instantaneous current draw of the PFC from the power line. The general form of the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times (V_{EA} - 0.7)}{V_{RMS}^{\ 2}} \times K \qquad (1)$$

Note that the output current of the gain modulator is limited around 159μA and the maximum output voltage of the gain modulator is limited to 159μA x 5.7K=0.906V. This 0.906V also determines the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. $I_{SENSE}=I_{GAINMOD} – I_{OFFSET}$ and I_{OFFSET} can only be measured when V_{EA} is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 31μA ~ 48μA.

Selecting R_{AC} for IAC Pin

The IAC pin is the input of the gain modulator and also a current mirror input and requires current input. Selecting a proper resistor R_{AC} provides a good sine wave current derived from the line voltage and helps program the maximum input power and minimum input line voltage. $R_{AC}=V_{IN}$ peak x 56KΩ. For example, if the minimum line voltage is $75V_{AC}$, the R_{AC}=75 x 1.414 x 56KΩ=6MΩ.

Current Amplifier Error, IEA

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current, which results in a negative voltage being impressed upon the ISENSE pin.

The negative voltage on ISENSE represents the sum of all currents flowing in the PFC circuit and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

The inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator causes the output stage to increase its duty cycle until the voltage on ISENSE is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle decreases to achieve a less negative voltage on the ISENSE pin.

PFC Cycle-By-Cycle Current Limiter

As well as being a part of the current feedback loop, the ISENSE pin is a direct input to the cycle-by-cycle current limiter for the PFC section. If the input voltage at this pin is less than -1.15V, the output of the PFC is disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the FAN4800A/C, FAN4801/1S/2/2L includes TriFault Detect. This feature monitors FBPFC for certain PFC fault conditions.

In a feedback path failure, the output of the PFC could exceed safe operating limits. With such a failure, FBPFC exceeds its normal operating area. Should FBPFC go too LOW, too HIGH, or OPEN, TriFault Detect senses the error and terminates the PFC output drive.

TriFault detect is an entirely internal circuit. It requires no external components to serve its protective function.

PFC Over-Voltage Protection

In the FAN4800A/C, FAN4801/1S/2/2L, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high-voltage DC output of the PFC is fed to FBPFC. When the voltage on FBPFC exceeds 2.75V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 250mV of hysteresis and the PFC does not restart until the voltage at FBPFC drops below 2.50V. V_{DD} OVP can also serve as a redundant PFC OVP protection. V_{DD} OVP threshold is 28V with 1V hysteresis.

Selecting PFC R_{sense}

R_{SENSE} is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_{SENSE} equals $I_{GAINMOD}$ x 5.7KΩ.

At full load, the average V_{EA} needs to around 4.5V and ripple on the V_{EA} needs to be less than 400mV. Choose the resistance of the sensing resistor:

$$R_{SENSE} = \frac{(4.5-0.7)\times 5.7K\Omega \times I_{AC} \times Gain \times V_{IN} \times \sqrt{2}}{2\times(5.6-0.7)\times Line\ Input\ Power} \qquad (2)$$

where 5.6 is V_{EA} maximum output.

PFC Soft-Start

PFC startup is controlled by V_{EA} level. Before FBPFC voltage reaches 2.4V, the V_{EA} level is around 2.8V. At $90V_{AC}$, the PFC soft-start time is 90ms.

PFC Brownout

The AC UVP comparator monitors the AC input voltage. The FAN4800A/C, FAN4801/1S/2 disables OPFC when the VRMS is less than 1.05V and continues 500ms. The VRMS threshold low voltage of FAN4802L is 0.9V, which is different from the FAN4802.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor because an increase in the input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 45 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current-loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: As the reference voltage increases from 0V, it creates a differentiated voltage on I_{EA}, which prevents the PFC from immediately demanding a full duty cycle on its boost converter. *Complete design is referred in application note AN-6078SC.*

There is an RC filter between R_{SENSE} and ISENSE pin. There are two reasons to add a filter at the ISENSE pin:

1. Protection: During startup or inrush current conditions, there is a large voltage across R_{SENSE}, which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} filter to attenuate the energy.
2. To reduce L, the boost inductor: The I_{SENSE} filter also can reduce the boost inductor value since the I_{SENSE} filter behaves like an integrator before the ISENSE pin, which is the input of the current error amplifier, I_{EA}.

The I_{SENSE} filter is an RC filter. The resistor value of the I_{SENSE} filter is between 100Ω and 50Ω because I_{OFFSET} x R_{FILTER} can generate a negative offset voltage of IEA. Selecting an R_{FILTER} equal to 50Ω keeps the offset of the I_{EA} less than 3mV. Design the pole of I_{SENSE} filter at $f_{PFC}/6$, one sixth of the PFC switching frequency, so the boost inductor can be reduced six times without disturbing the stability. The capacitor of the I_{SENSE} filter, C_{FILTER}, is approximately 100nF.

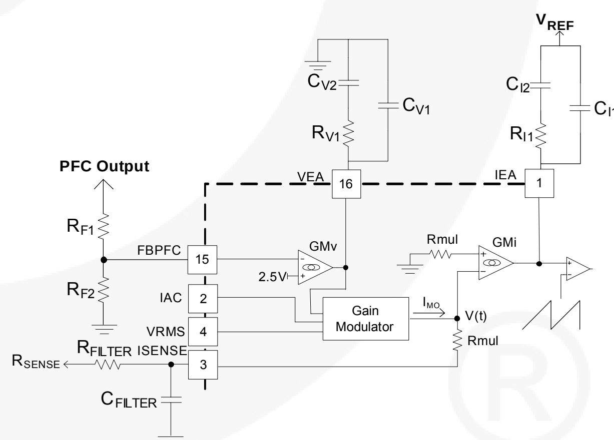


Figure 45. Compensation Network Connection for the Voltage and Current Error Amplifiers

Two-Level PFC Function

To improve the efficiency, the system can reduce PFC switching loss at low line and light load by reducing the PFC output voltage. The two-level PFC output of FAN4801/1S/2/2L can be programmable.

As Figure 46 shows, FAN4801/1S/2/2L detect VEA pin and VRMS pin to determine the system operates low line and light load or not. At the second-level PFC, there is a current of 20µA through R_{F2} from FBPFC pin. So the second-level PFC output voltage can be calculated as.

$$Output \cong \frac{R_{F1}+R_{F2}}{R_{F2}} \times (2.5V - 20\mu A \times R_{F2}) \quad (3)$$

For example, if the second-level PFC output voltage is expected as 300V and normal voltage is 387V, according to the equation, R_{F2} is 28kΩ R_{F1} is 4.3MΩ.

The programmable range of second level PFC output voltage is 340V ~ 300V.

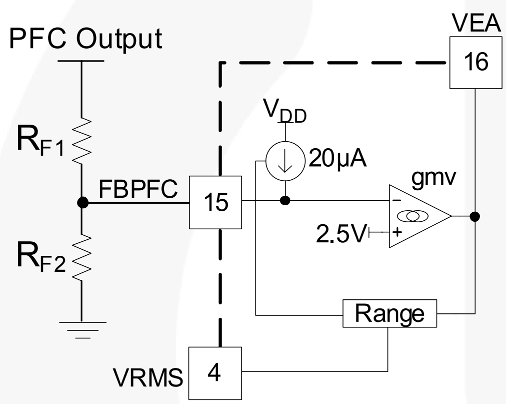


Figure 46. Two-Level PFC Scheme

Oscillator (R_T/C_T)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the oscillator output clock:

$$f_{RT/CT} = \frac{1}{t_{RT/CT} + t_{DEAD}} \quad (4)$$

The dead time of the oscillator is derived from the following equation:

$$t_{RT/CT} = C_T \times R_T \times \ln\left(\frac{V_{REF}-1}{V_{REF}-3.8}\right) \quad (5)$$

at V_{REF}=7.5V and $t_{RT/CT}=C_T \times R_T \times 0.56$.

The dead time of the oscillator is determined using:

$$t_{DEAD} = \frac{2.8V}{7.78mA} \times C_T = 360 \times C_T \quad (6)$$

The dead time is so small ($t_{RT/CT} >> t_{DEAD}$) that the operating frequency can typically be approximated by:

$$f_{RT/CT} = \frac{1}{t_{RT/CT}} \quad (7)$$

Pulse Width Modulator (PWM)

The operation of the PWM section is straightforward, but there are several points that should be noted. Foremost among these is the inherent synchronization of PWM with the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage. It is thereby representative of the current flowing in the converter's output stage. I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP in such applications. For voltage-mode operation and certain specialized applications, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which FBPWM is compared. Under these conditions, the use of voltage feed-forward from the PFC bus can assist in line regulation accuracy and response. As in current-mode operation, the I_{LIMIT} input is used for output stage over-current protection. No voltage error amplifier is included in the PWM stage, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of opto-coupler feedback circuitry, an offset has been built into the PWM's RAMP input that allows FBPWM to command a 0% duty cycle for input voltages below typical 1.5V.

PWM Cycle-By-Cycle Current Limiter

The ILIMIT pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. When the I_{LIMIT} triggers the cycle-by-cycle bi-cycle current, it limits the PWM duty cycle mode and the power dissipation is reduced during the dead-short condition.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if the voltage on FBPFC is less than its nominal 2.4V. Once the voltage reaches 2.4V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

PWM Soft-Start (SS)

PWM startup is controlled by selection of the external capacitor at soft-start. A current source of 10µA supplies the charging current for the capacitor and startup of the PWM begins at 1.5V.

PWM Control (RAMP)

When the PWM section is used in current mode, RAMP is generally used as the sampling point for a voltage, representing the current in the primary of the PWM's output transformer. The voltage is derived either from a current sensing resistor or a current transformer. In voltage mode, RAMP is the input for a ramp voltage generated by a second set of timing components (R_{RAMP}, C_{RAMP}) that have a minimum value of 0V and a peak value of approximately 6V. In voltage mode, feed forward from the PFC output bus is an excellent way to derive the timing ramp for the PWM stage.

Generating V_{DD}

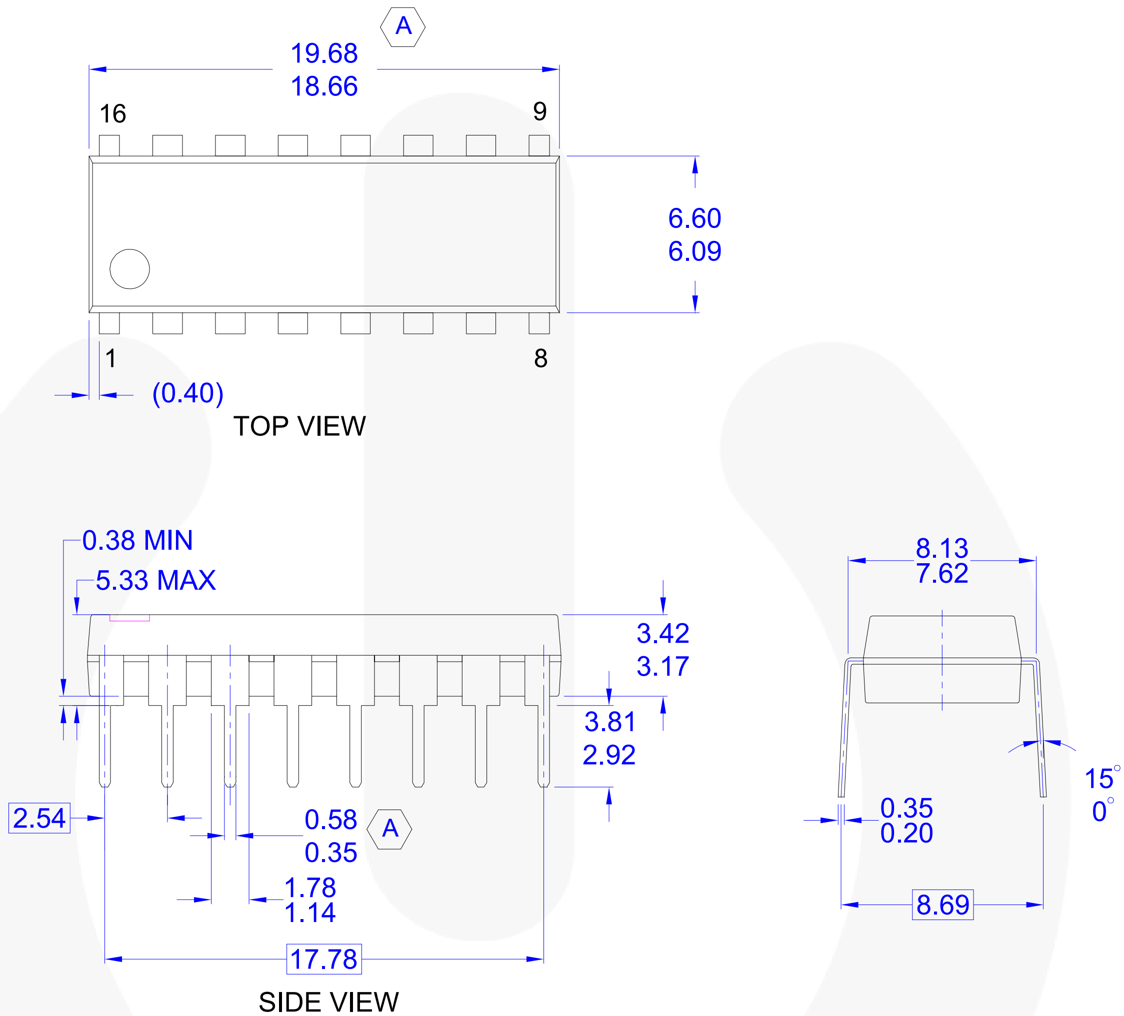
After turning on the FAN4800A/C, FAN4801/1S/2/2L at 11V, the operating voltage can vary from 9.3V to 28V. The threshold voltage of the V_{DD} OVP comparator is 28V and its hysteresis is 1V. When V_{DD} reaches 28V, OPFC is LOW, and the PWM section is not disturbed. There are two ways to generate V_{DD}: use auxiliary power supply around 15V or use bootstrap winding to self-bias the FAN4800A/C, FAN4801/1S/2/2L system. The bootstrap winding can be taped from the PFC boost choke or the transformer of the DC-to-DC stage.

Leading/Trailing Modulation

Conventional PWM techniques employ trailing-edge modulation, in which the switch turns on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on-time of the switch.

In the case of leading-edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty-cycle of the leading-edge modulation is determined during off-time of the switch.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

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B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS

D) CONFORMS TO ASME Y14.5M-1994

E) DRAWING FILE NAME: N16EREV1

Figure 47. 16-Pin Dual In-Line Package (DIP)

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Physical Dimensions (Continued)

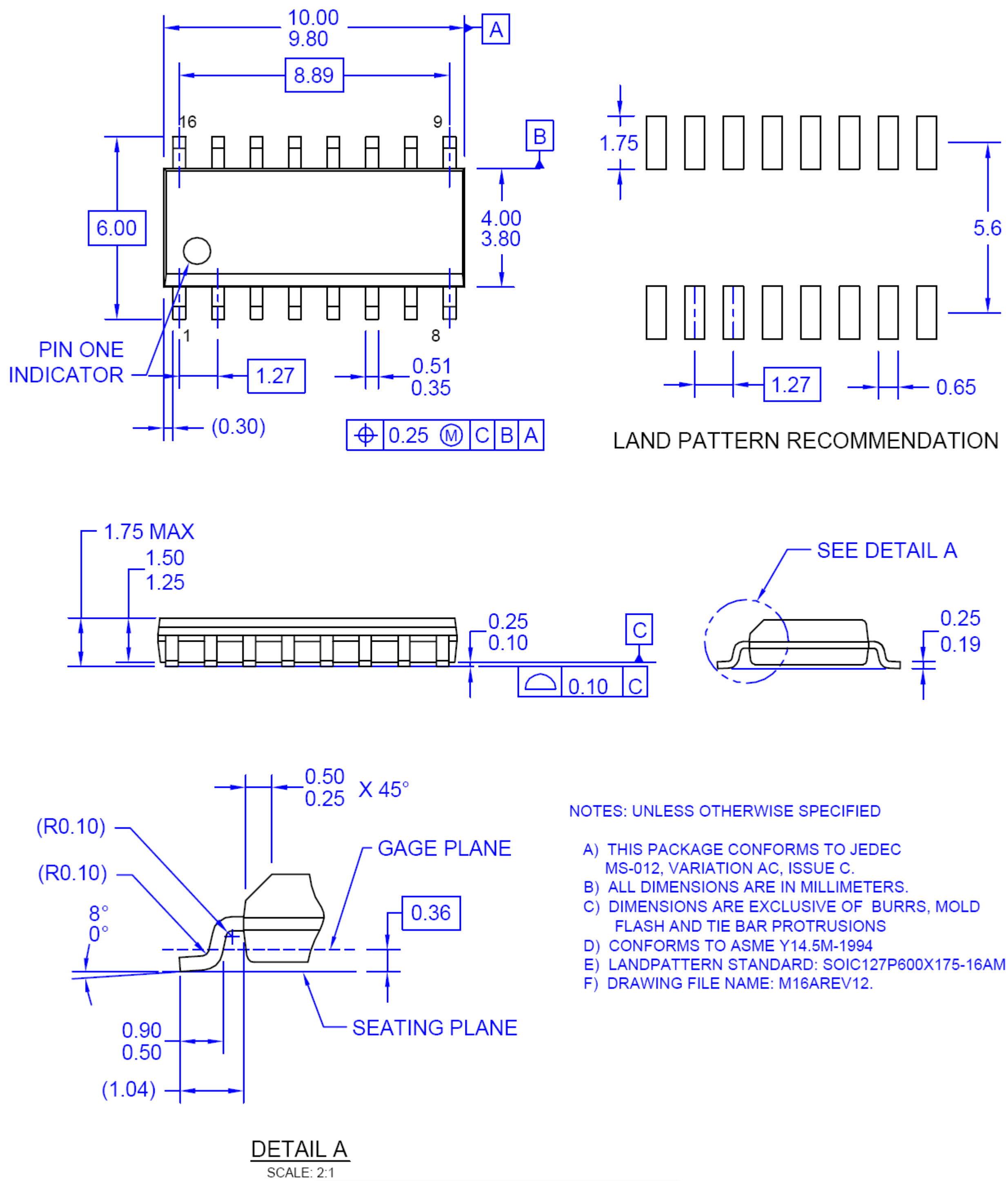

Figure 48. 16-Pin Small Outline Package (SOIC)

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Rev. I40